"Predicting Long-Term Electromagnetic Robustness of Integrated Circuits based on the Accelerated Degradation Test (ALT)"

January 14, 2023

Supervisors:
Laurent Saintis, LARIS, Polytech Angers, Francce
Mohsen Koohestani, ESEO, Angers, France
Mihaela Barreau, LARIS, Polytech Angers, France

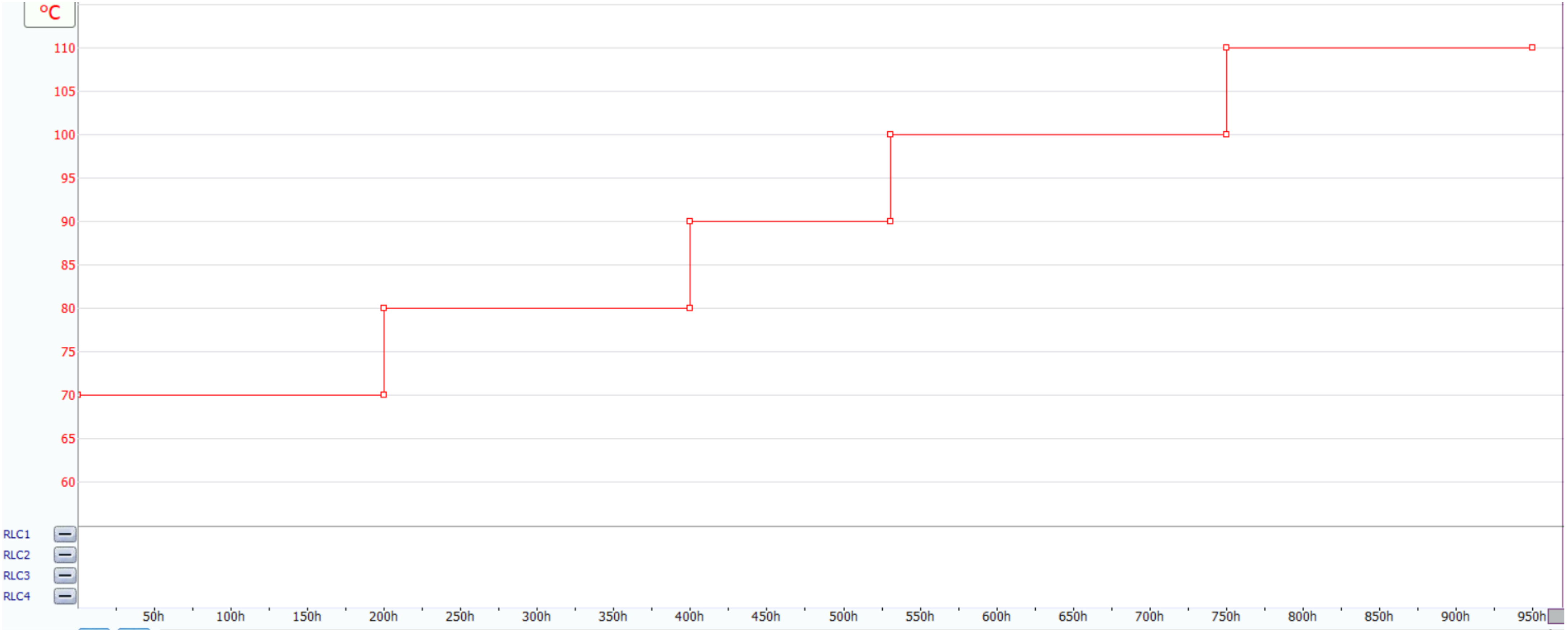
Presented by:
MD JABER AL RASHID
mdjaberal.rashid@etud.univ-angers.fr
(LARIS, POYTECH ANGERS, FRANCE)

Outline of the presentation

- ❑ Design of ADT (accelerated degradation test plan)
- ❑ Experimental setup and methodology for accelerated ageing test
- ❑ EMC performance test results for UA78L05 (i.e. sample T 1)
- ❑ **ADT degradation path curve for IC regulators (i.e. UA78L05 and L78L05) in high frequency** FREQUENCY RANGE
- ❑ **ADT degradation path model**
  - Physics based model
  - Gamma process
- ❑ Conclusion and Future Perspective

Design of ADT test plan (Programmed in climatic chamber)

- Total stress time duration: 950 hours
- Thermal step-stress: 70 °C-110 °C with step size of 10 °C
- Electrical stress: 9 V and 12 V

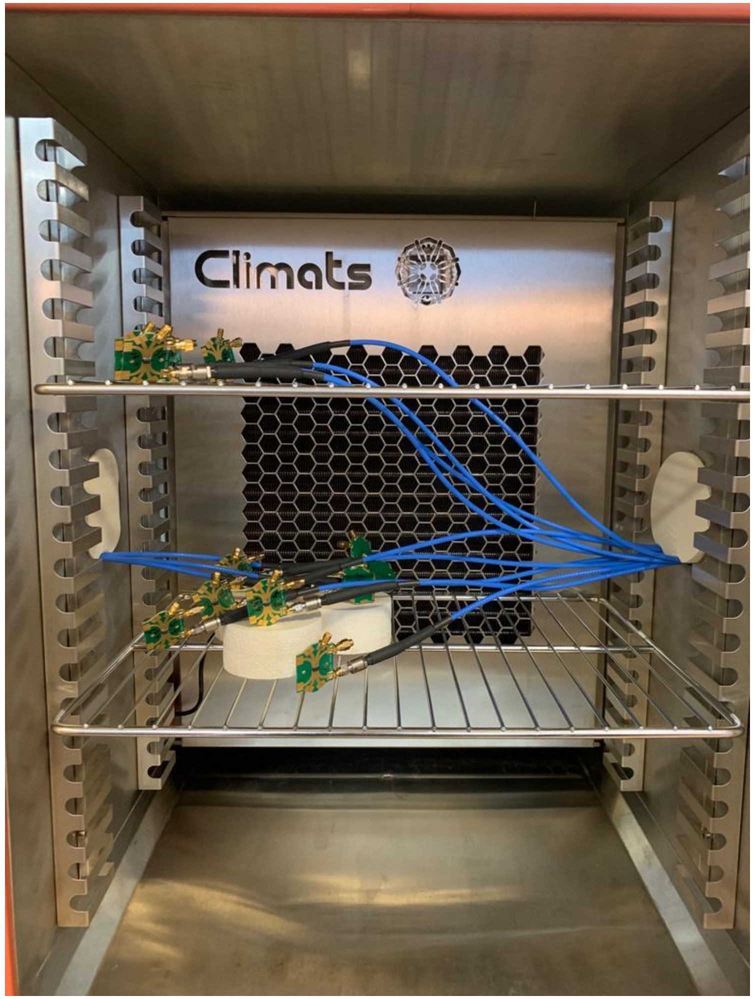


Accelerated ageing stress conditions for the SSADT on ICs

IC reference	Samples	Thermal stress (°C)	Electrical overstress (V)	Total stress duration (hours)
UA78L05	3 units (T1, T2 and T3)	70-110 °C	9 V	950 hours
	3 units (T4, T5 and T6)	70-110 °C	12 V	950 hours
L78L05	3 units (S1, S2 and S3)	70-110 °C	9 V	950 hours
	3 units (S1, S2 and S3)	70-110 °C	12 V	950 hours

Experimental setup for accelerated ageing test

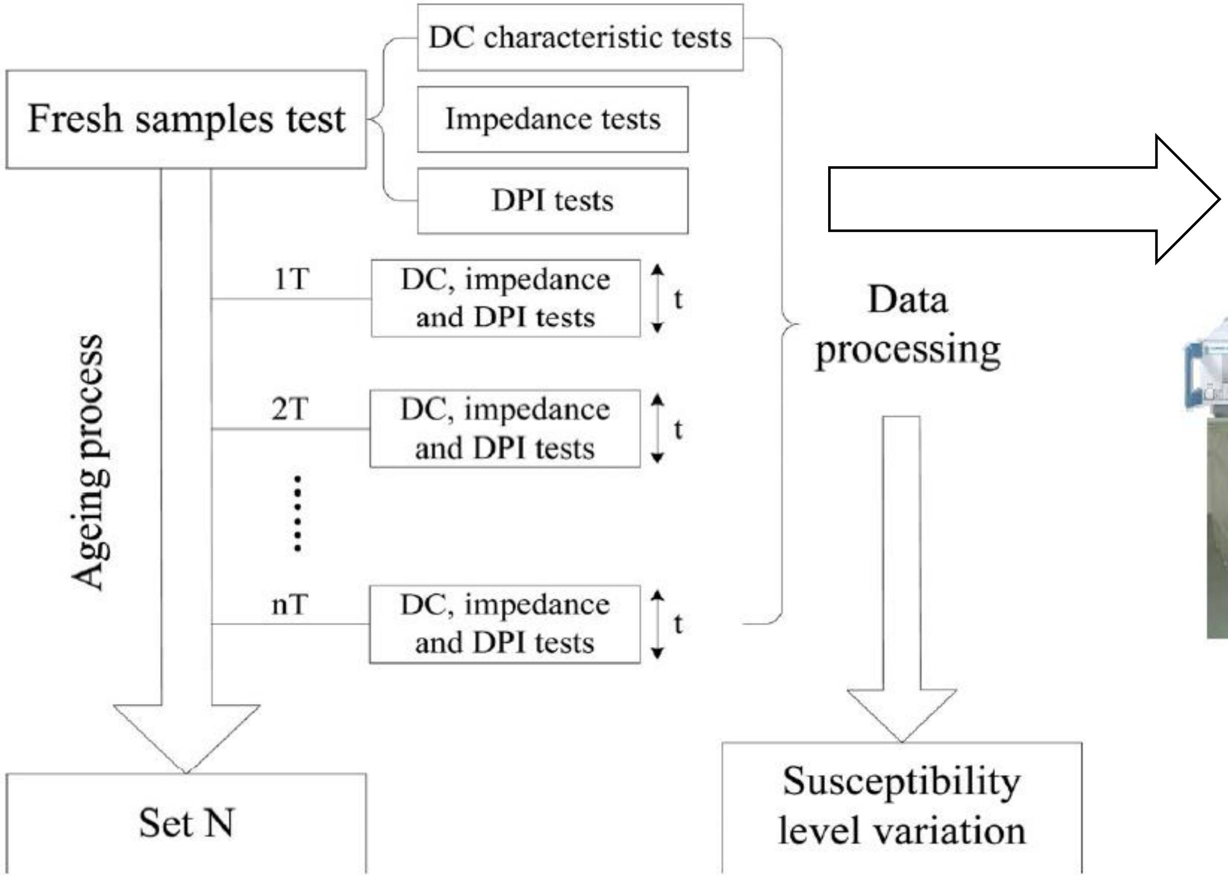
Device under tests inside the climatic chamber



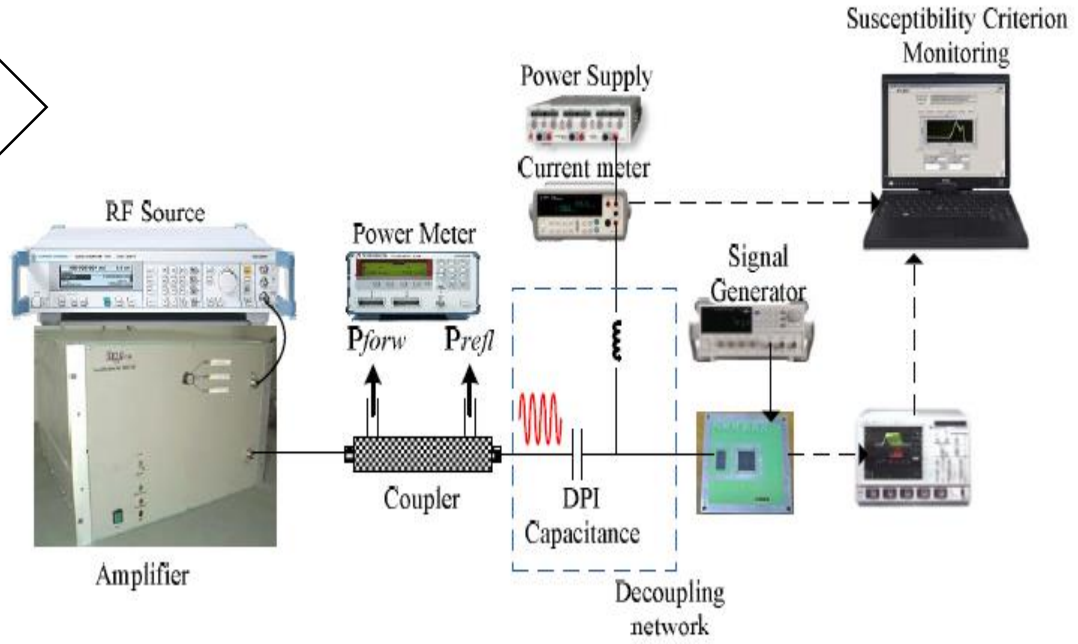
Climatic chamber for accelerated ageing test

Experimental Procedure: Characterize the EMC performance immunity drift accelerated ageing test

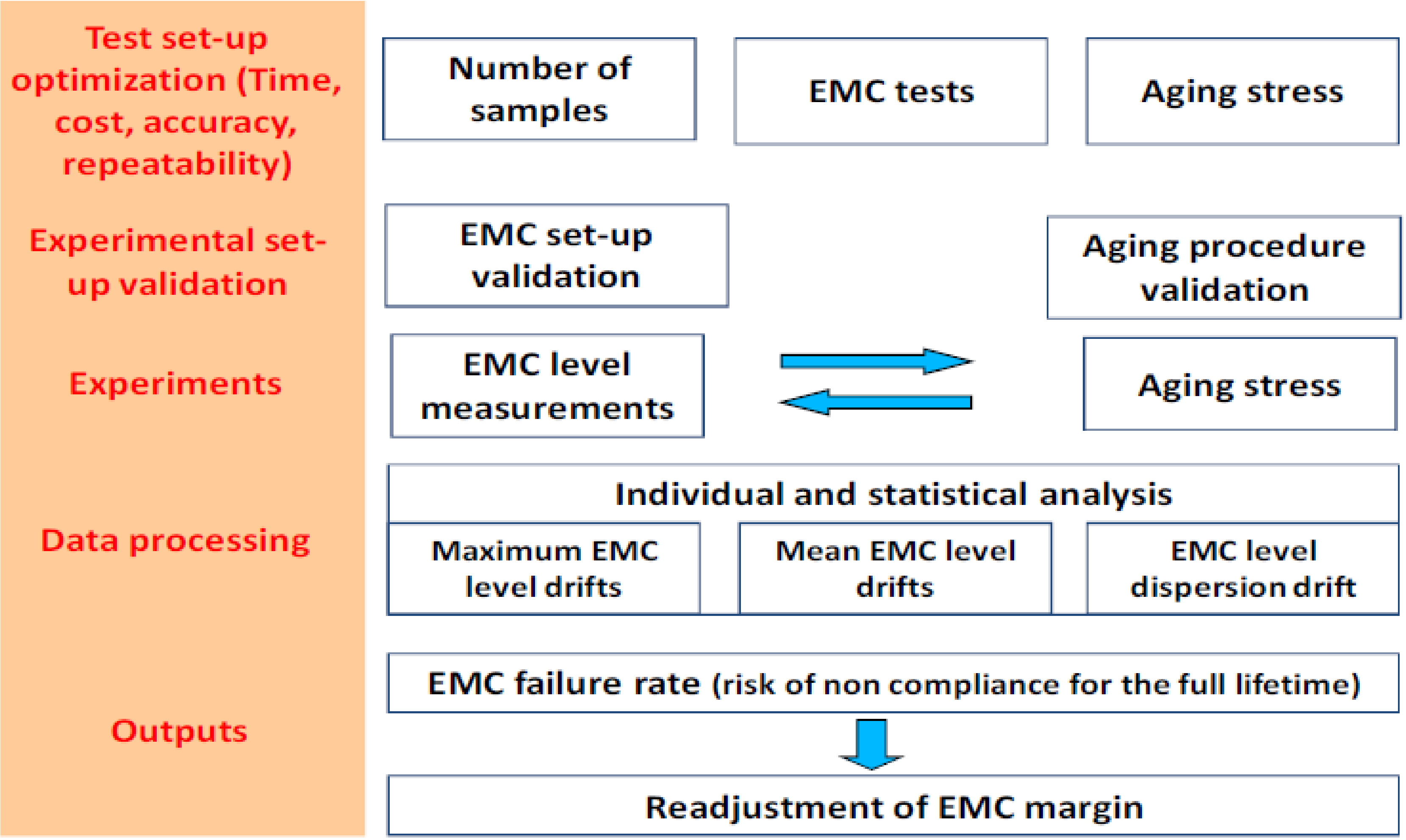
Frequency dependent accelerated ageing methodology



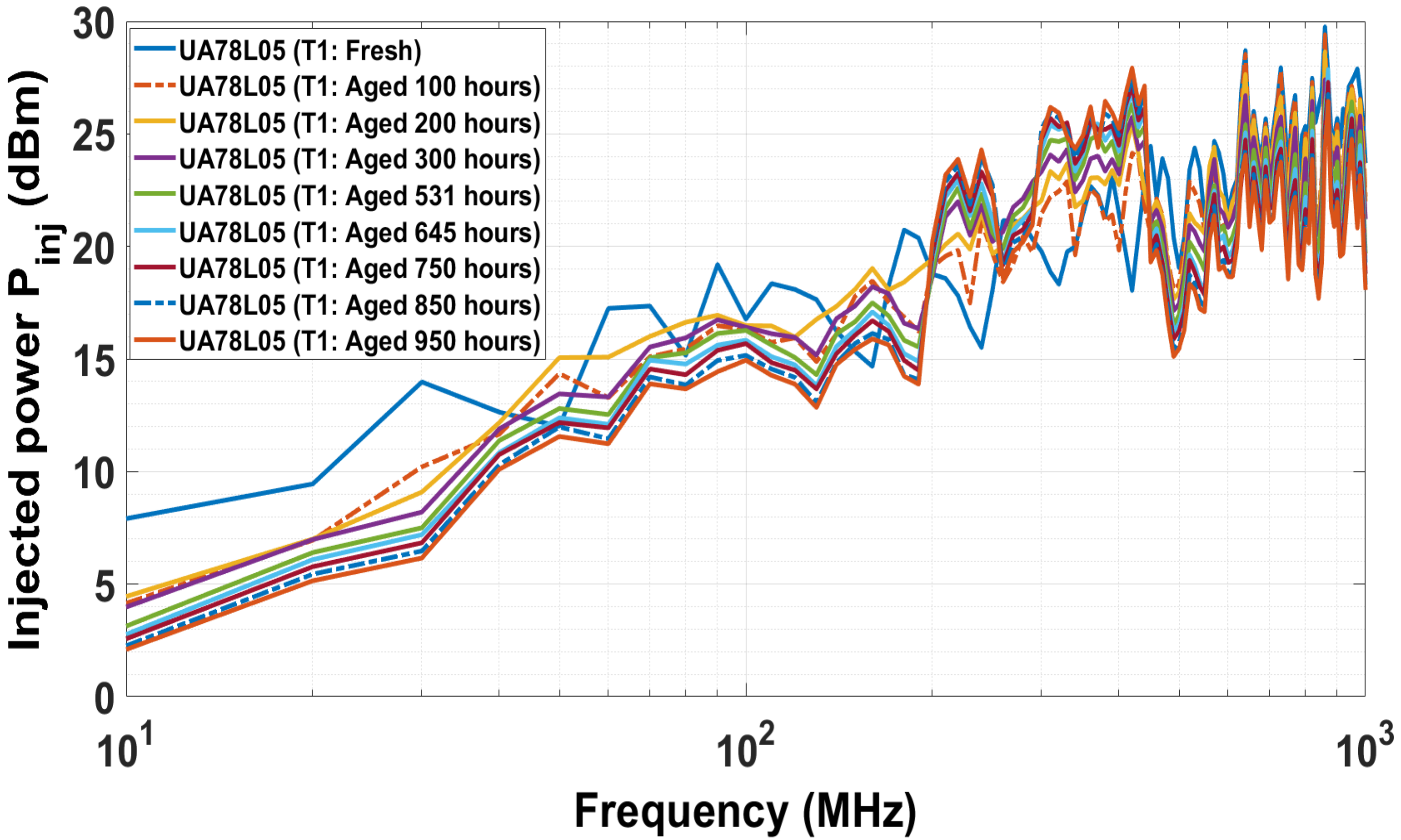
Direct power injection (DPI) set up for EMC performance measurement before and after ageing



Methodology: Characterizing the electromagnetic robustness (EMR) of ICs under the accelerated ageing test



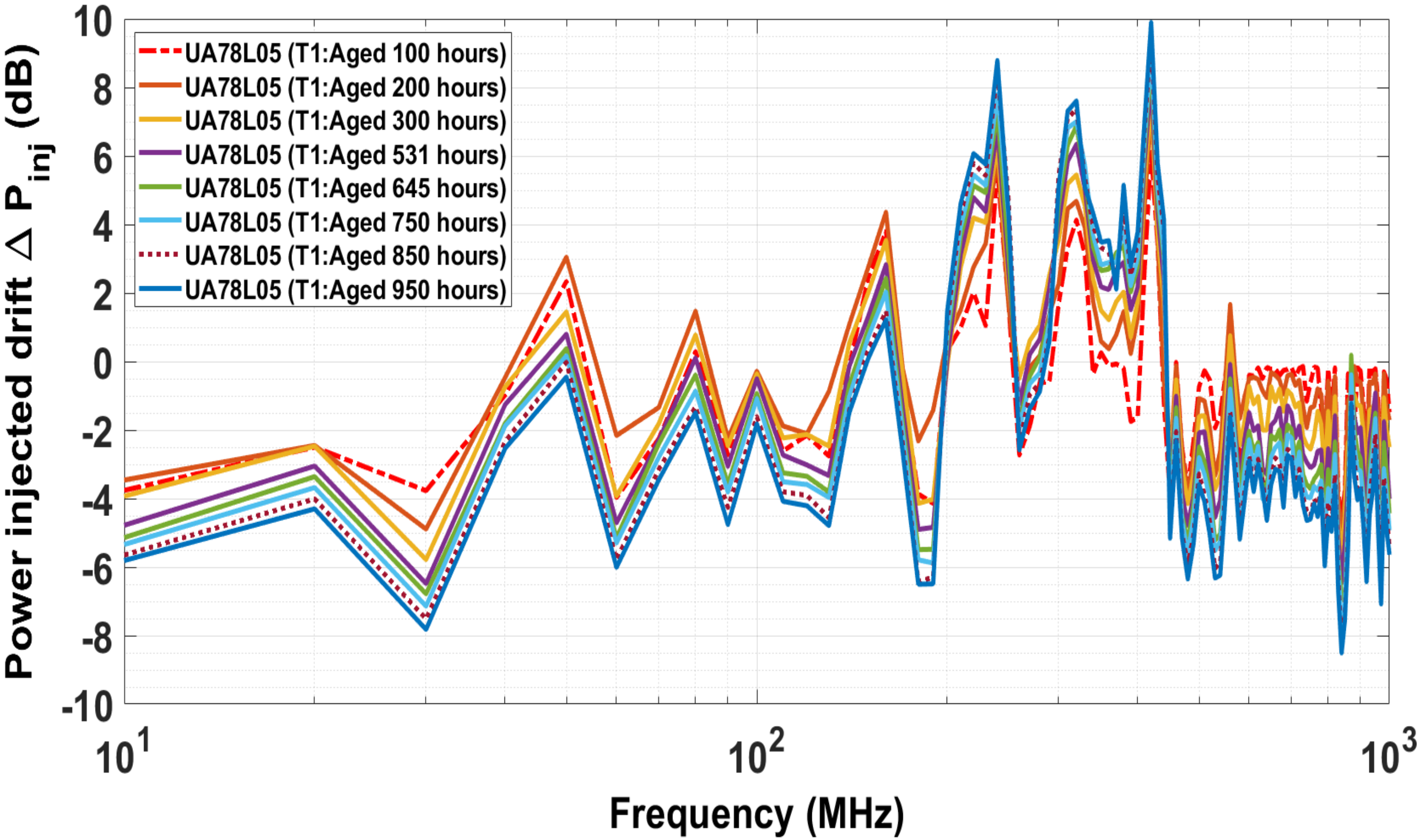
DPI performance of aged IC regulators (sample T 1: UA78L05) upto 950 hours



- ❑ Aged IC (L78L05) regulator showed decrease in EMC performance with increase in ageing time.
- ❑ EMC ageing immunity drift can be calculated by subtracting injected power before ageing from the injected power after ageing

$$\Delta_M = \frac{1}{N_{sample}} \sum_{i=1}^{N} (X_{Ai} - X_{Bi})$$

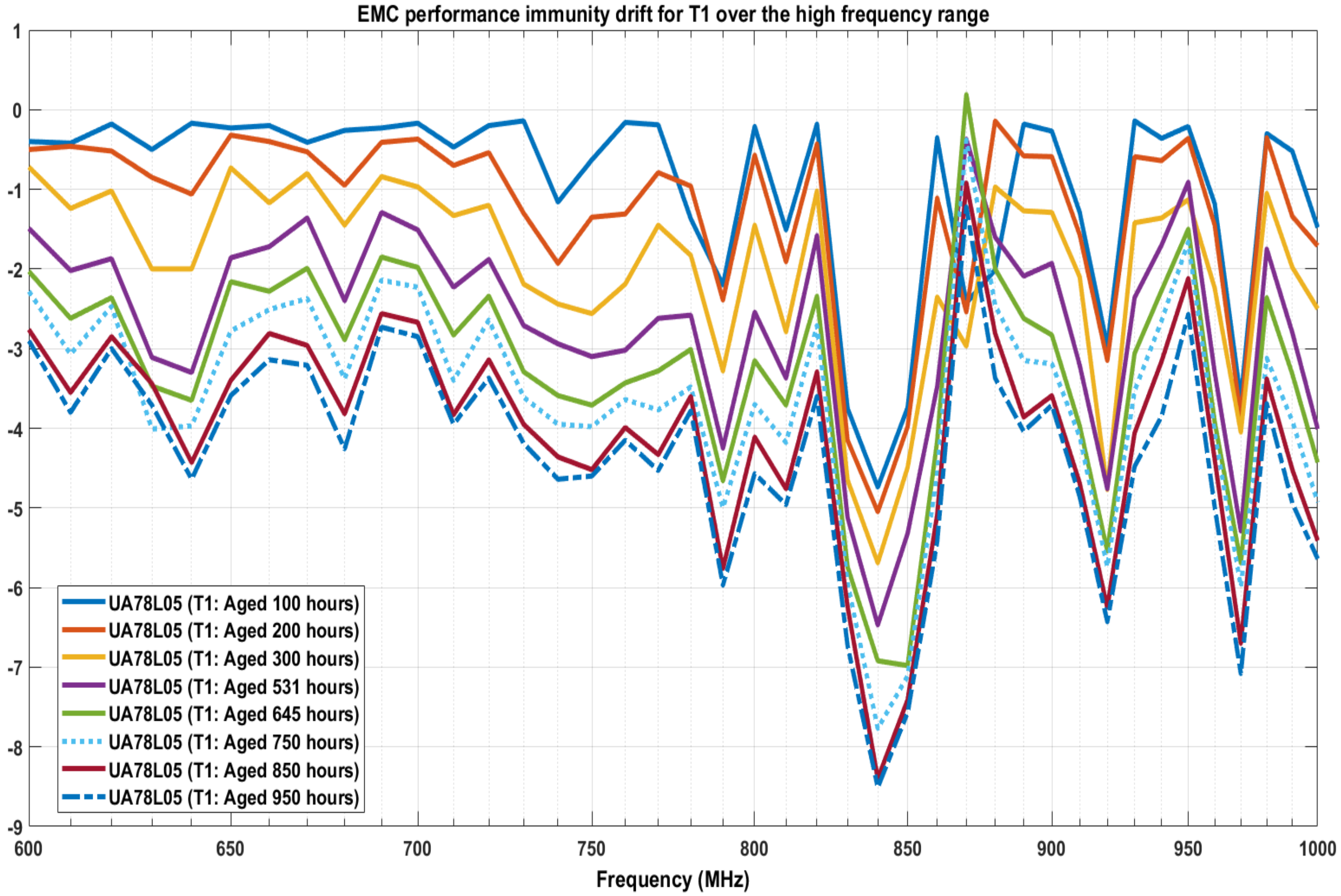
EMC performance indicator (i.e. Power injection drift) of aged IC (sample T 1: UA78L05) over the whole frequency range upto 950 hours



- Aged IC (UA78L05) regulator sample (i.e. T1) showed varying power injected drift for different frequencies at different ageing stess time.
- Positive value for the power injection drift means improvement in immunity and vice versa.
- It is possible to calculate the immunity drift by subtracting power injected after ageing from power injected before ageing.

$$\Delta_M = \frac{1}{N_{sample}} \sum_{i=1}^{N} (X_{Ai} - X_{Bi})$$

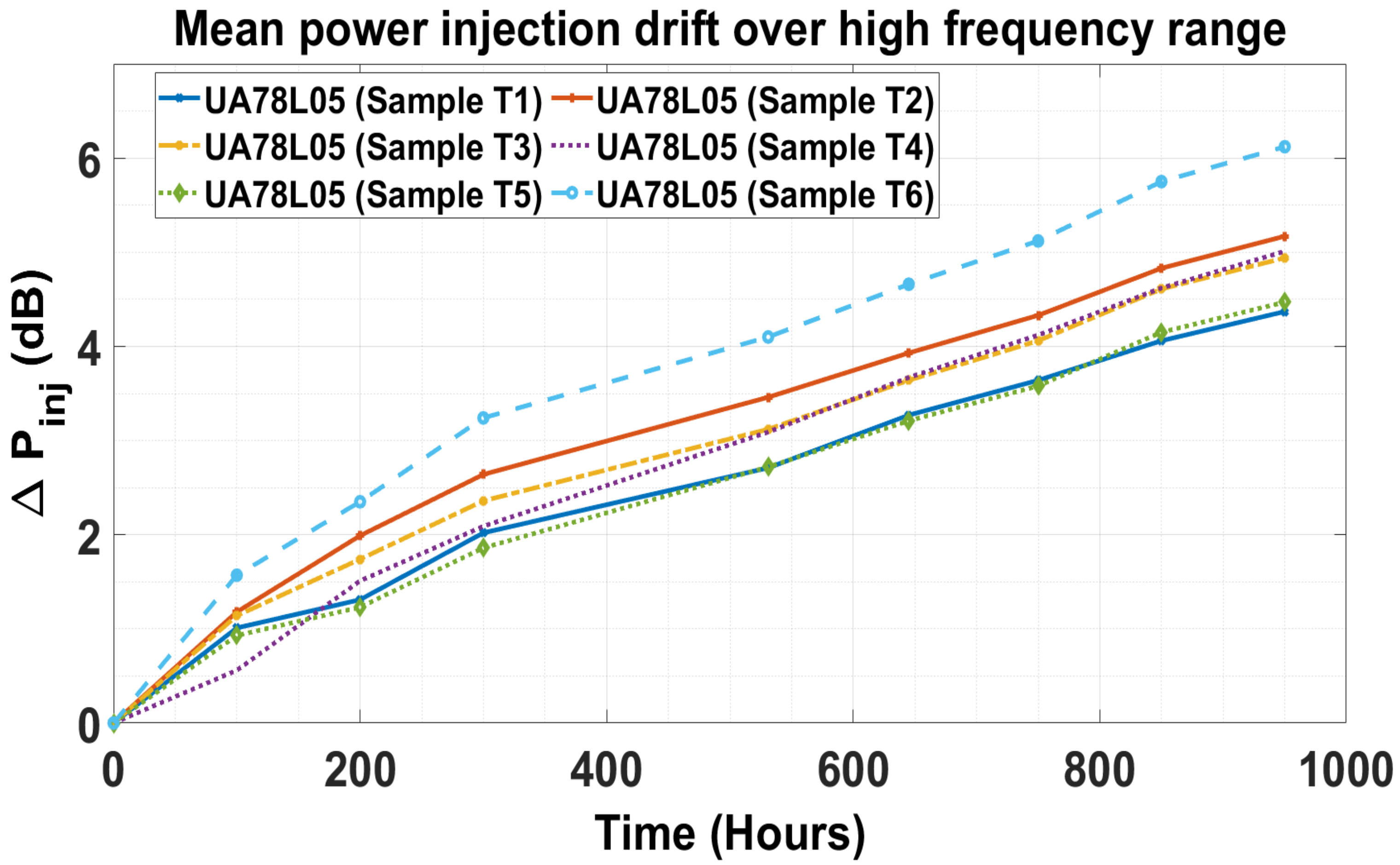
EMC performance indicator (i.e. Power injection drift) of aged IC (sample T 1: UA78L05) over the high frequency range



- Aged IC (UA78L05) regulator sample (i.e. T1) showed varying power injected drift for different frequencies at different ageing stess time.
- Negative value for the power injection drift means conducted immunity after ageing reduced.
- It is possible to calculate the immunity drift by subtracting power injected after ageing from power injected before ageing.

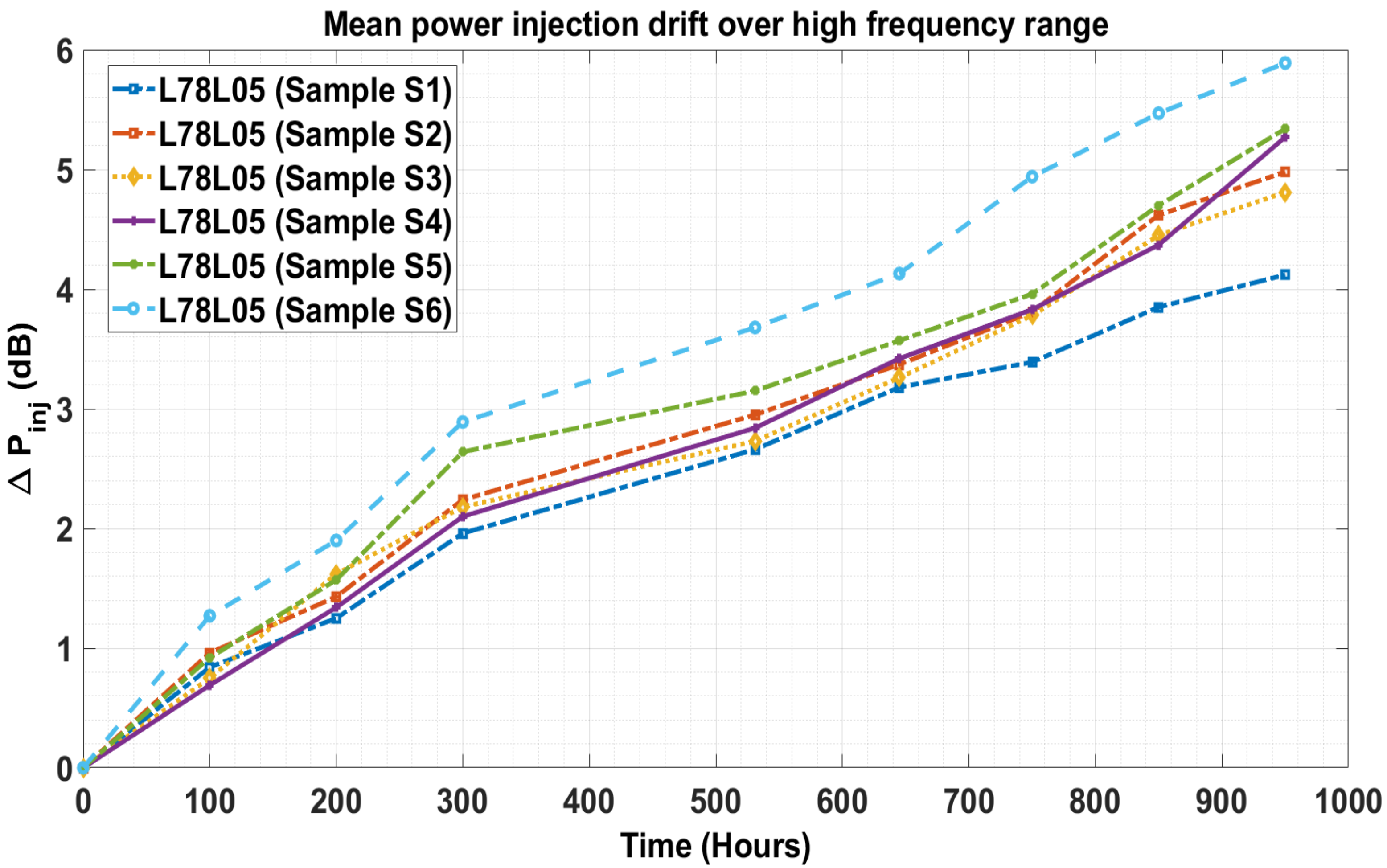
$$\Delta_M = \frac{1}{N_{sample}} \sum_{i=1}^{N} (X_{Ai} - X_{Bi})$$

Degradation profile curves for UA78L05 over high frequency range (i.e. 600-1000 MHz)



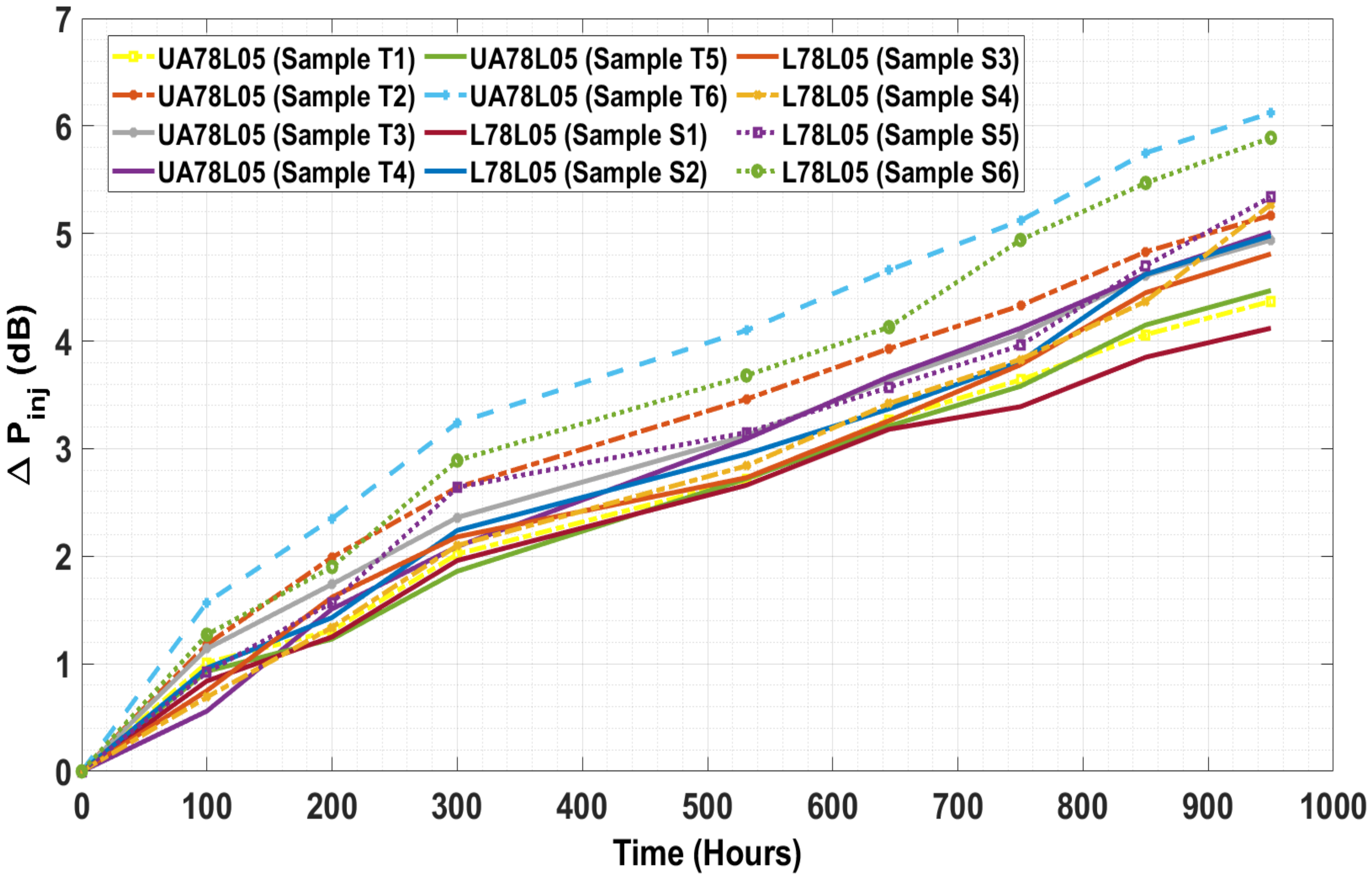
- ❑ Aged ICs (UA78L05) regulator showed increase in EMC performance degradation with increase in ageing time for high frequency range.
- ❑ Monotonic degradation is observed at high frequency range between 600 and 1000 MHz.
- ❑ Mean power injection drift (Δpinj) increases with increase in stress duration, which means the conducted immunity reduces due to ageing.

Degradation profile curves for L78L05 over high frequency range (i.e. 600-1000 MHz)



- Aged IC (L78L05) regulator showed slight increase in EMC performance degradation with increase in ageing time.
- S4, S5 and S6 showed high mean immunity drift for high thermal and electrical stress.

Comparing degradation profile curves for UA78L05 & L78L05 over high frequency range (i.e. 600-1000 MHz)



- Aged IC (L78L05) regulator showed less increase in EMC performance degradation compared to that of UA78L05 with increase in ageing time.
- Power injection immunity drift is found to be higher for UA78L05 compared to that of L78L05.
- Samples (i.e. T 1, T 2 and T 3) of UA78L05 aged at low electrical voltage stress condition showed less immunity drift compared to that of other 3 samples (i.e. T4, T5 and T6).

Physics-based model

- **Expression of the degradation function g of stress and time**

$$g(t) = A \times t^{\gamma}$$

$\ln\left(\frac{\Delta P_{\{inj\}}}{P_{inj}}\right) = \ln(A_{ikl}) + \gamma \ln(t)$ for component i, level of input voltage k and level of temperature

- **Expression of acceleration law**

$$L = \frac{A}{V^B} \exp\left(\frac{E_a}{KT}\right)$$

$$A_{ikl} = \frac{\alpha_i}{V^B} \exp\left(\frac{E_a}{KT}\right) \Rightarrow \ln(A_{ikl}) = \ln(\alpha_i) - B.\ln(V) + \frac{E_a}{KT}$$

- **General Analytic expression for the cumulative distribution function (CDF) for one value of stress**

$$F_{kl}(t) = \Pr(g(t, S_{kl}) \geq G) = \Pr\left(\beta_1 + \beta_2.\ln(V) + \beta_3.\frac{1}{T} + \beta_4 .\ln(t) \geq \ln(G)\right)$$

$$= \Phi\left(\frac{\ln(G) - \beta_2.\ln(V) - \beta_3.\frac{1}{T} - \beta_4 .\ln(t) - \mu_\alpha}{\sigma_\alpha}\right) \quad \textit{with } \Phi \textit{ the cdf of standard normal distribution}$$

Degradation path model for the SSADT on the IC regulators

Physics-based model:

- Likelihood expression for the probability distribution function for the step-stress ADT test

$$\ln\left(f_{ik}(t_i)\right)=\begin{cases} -\ln\left(\sigma_\alpha\sqrt{2\pi}\right)-\frac{1}{2}\left(\frac{\ln(G)-\beta_2.\ln(V)-\beta_3.\frac{1}{T_1}-\beta_4.\ln(t)-\mu_\alpha}{\sigma_\alpha}\right)^2 & for\ 0<t<t_1\ ,at\ \ T_1=S_1=70\,°C\ ;\ \ 0<t\le 200\ hours \\ -\ln\left(\sigma_\alpha\sqrt{2\pi}\right)-\frac{1}{2}\left(\frac{\ln(G)-\beta_2.\ln(V)-\beta_3.\frac{1}{T_2}-\beta_4.\ln(w_2+t-t_1)-\mu_\alpha}{\sigma_\alpha}\right)^2 & for\ t_1<t<t_2\ ,at\ \ T_2=S_2=80\,°C;\ \ 200<t\le 400\ hours \\ -\ln\left(\sigma_\alpha\sqrt{2\pi}\right)-\frac{1}{2}\left(\frac{\ln(G)-\beta_2.\ln(V)-\beta_3.\frac{1}{T_3}-\beta_4.\ln(w_3+t-t_2)-\mu_\alpha}{\sigma_\alpha}\right)^2 & for\ t_2<t<t_3\ ,at\ \ T_3=S_3=90\,°C\ ;\ 400<t\le 531\ hours \\ \vdots & \\ -\ln\left(\sigma_\alpha\sqrt{2\pi}\right)-\frac{1}{2}\left(\frac{\ln(G)-\beta_2.\ln(V)-\beta_3.\frac{1}{T_4}-\beta_4.\ln(w_4+t-t_3)-\mu_\alpha}{\sigma_\alpha}\right)^2 & for\ t_3<t<t_4\ ,at\ \ T_4=S_4=100\,°C\ ;\ 531<t\le 750\ hours \\ \ln\left(\sigma_\alpha\sqrt{2\pi}\right)-\frac{1}{2}\left(\frac{\ln(G)-\beta_2.\ln(V)-\beta_3.\frac{1}{T_5}-\beta_4.\ln(w_5+t-t_4)-\mu_\alpha}{\sigma_\alpha}\right)^2 & for\ t_4<t<t_5\ ,at\ \ T_5=S_5=110\,°C\ ;\ \ 750<t\le 950\ hours \end{cases}$$

- Expression for the applying Maximum Likelihood estimation (MLE) method

$$\ln\left(\mathcal{L}(t/\mu_\alpha,\sigma_\alpha,\beta_2,\beta_3,\beta_4)\right)=\sum_{k=1}^{2}\sum_{i=1}^{n_k}\ln\left(f_{ik}(t_i)\right)$$

Degradation path model for the SSADT on the IC regulators

❑ Gamma-process (i.e. Statistical model)

❑ *Analytic expression of a Gamma process for degradation with acceleration law*

➢ $g(\tau_j) = \mu_{ikl}(t+1) - \mu_{ikl}(t) = \ln\left(\frac{\Delta P_{\{inj\}}}{P_{inj}}\right) = \ln(A_{ikl}) + \gamma\ln(t)$ for component i, level of input voltage k and level of temperature l

❑ *Degradation path for the SSADT test on ICs*

$$\mu_{ik}(t) = \begin{cases} \mu_{ik1}(t) & 0 < t < t_1 \\ \mu_{ik2}(w_2 + t - t_1) & t_1 < t < t_2 \quad with\ \mu_{ik2}(w_2) = \mu_{ik1}(t_1) \Rightarrow w_2 = t_1 \times \exp\left(\frac{\beta_3}{\beta_4}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \\ \mu_{ik3}(w_3 + t - t_2) & t_2 < t < t_3 \quad with\ \mu_{ik3}(w_3) = \mu_{ik2}(w_2 + t_2 - t_1) \\ \vdots & \\ \mu_{ikm}(w_m + t - t_{(m-1)}) & t_{(m-1)} < t < t_m \quad with\ \mu_{ikm}(w_m) = \mu_{ik(m-1)}(w_{(m-1)} + t_{(m-1)} - t_{(m-2)}) \end{cases}$$

❑ *Analytic expression of the likelihood for SSADT for the gamma-process model*

$$\mathcal{L}(\boldsymbol{\theta}) = \prod_{j=1}^{N}\left[\boldsymbol{g}(\boldsymbol{\tau_j};\boldsymbol{\theta})\prod_{i=1}^{M-1}\boldsymbol{f}(\Delta\boldsymbol{x_{i,j}};\boldsymbol{\tau_i},\boldsymbol{\theta})\right]\ ; where\ \boldsymbol{\theta}: \{\mu_\alpha, \sigma_\alpha, \beta_2, \beta_3, \beta_4\},$$

N=6 (samples), m= 8 (number of measurements)

Conclusion & Future perspective

- *Hightlights :*

  - Express or derive the degradation indicators on the conducted immunity of the tested DUTs under ADT.

  - Obtain the DPI immunity test results characterized under defined accelerated stress conditions.

  - High temperature accelerated ageing test affects the EMC performance of both UA78L05 and L78L05 causing significant degradations in the power injected for causing failure or malfunction of the IC pin.

  - EMC immunity or susceptibility drift occurs due to ageing process on DUTs, causing reduction in the conducted immunity profile after ageing.

- *Future goals and objectives :*

  - Obtain the reliabilty model based on the degradation process to estimate long term EMC performance of Integrated circuits.

  - Express the reliability model function on the applied environmental stress conditions (temperature and voltage)

  - Obtain reliability modeling function to predict EMC performance of ICs

Questions ??

MD JABER AL RASHID

Email:, mdjaberal.rashid@etud.univ-angers.fr

(LARIS, POYTECH ANGERS, FRANCE

ESEO, Angers, France)